



Attorney Docket No. SON-1622  
Date: August 25, 1999



ASSISTANT COMMISSIONER FOR PATENTS  
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of

Inventor: MASAYUKI IIDA

For: LIQUID CRYSTAL DISPLAY DEVICE

Enclosed are:

- ☒ Specification and Claim(s).
- ☒ Oath or Declaration (executed).
- ☒ Five sheet(s) of drawings.
- ☒ An assignment of the invention to Sony Corporation.
- ☒ Copy of one priority application(s).
- ☐ Associate Power of Attorney.

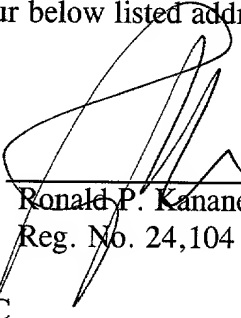
The fee has been calculated as shown below:

CLAIMS AS FILED				
FOR	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE \$380/\$760
TOTAL CLAIMS	6-20	0	X \$ 9 \$18	\$
INDEP. CLAIMS	2-3	0	X \$39 \$78	\$
Fee for Multiple Dependent Claims \$135/\$270				0
			TOTAL FILING FEE	\$760.00

- ☒ A Preliminary Amendment is attached.
- ☐ °Verified Statement claiming small entity status is enclosed.
- ☒ Charge \$ 760.00 to Deposit Account No. 18-0013 to cover the filing fee. A duplicate copy of this sheet is enclosed.
- ☒ The Commissioner is hereby authorized to charge any fees under 37 C.F.R. 1.16 or 1.17 which may be required during the entire pendency of this application, or to credit any overpayment, to Deposit Account No. 18-0013. A duplicate copy of this sheet is enclosed.
- ☐ A check in the amount of \$\_\_\_\_ cover the filing fee is enclosed.
- ☒ Charge \$ 40.00 to Deposit Account No. 18-0013 to cover the recordal fee. A duplicate copy of this sheet is enclosed.
- ☒ Applicant's undersigned attorney may be reached by telephone in our Washington D.C. Office at

(202) 955-3750.

All correspondence should be directed to our below listed address.

  
\_\_\_\_\_  
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Reg. No. 24,104

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Patent Application of

MASAYUKI IIDA

Serial No. (Not Yet Assigned)

Filed: August 25, 1999

For: LIQUID CRYSTAL DISPLAY DEVICE

ATTN: APPLICATION BRANCH

PRELIMINARY AMENDMENTAssistant Commissioner of Patents  
Washington, DC 20231

Sir:

Prior to the initial examination, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 1, line 9, change "Hitherto, there is known a liquid crystal display device" to -- A liquid crystal display device is known--.

Page 1, line 13, change "etc." to -- and so forth --.

Page 1, line 20, change "quartz substrate, etc." to -- a quartz substrate, and so forth --.

Page 3, line 7, before "quartz" insert an -- a --.

Page 3, line 8, before "second" insert -- i.e., a --.

Page 3, lines 9 and 10 change "DOPOS (a gate insulating film 31 made of, for example, SiO<sub>2</sub> intervenes between them)" to -- DOPOS, in which a gate insulating film 31 made of, for example, SiO<sub>2</sub> intervenes between them --.

Page 3, line 19, after "under" insert -- or beneath --.

Page 3, line 20, after "line" (second occurrence) insert -- 4 --.

Page 4, line 2, change "of" to -- by --.

Page 4, line 4, change "Incidentally, in Figs." to -- In Figs. --

Page 4, line 5, after "contact"(both occurrences), change the comma "," to a semicolon -- ; --.

Page 4, line 6, after "A1", change the comma "," to a semicolon --; --; and after "portion", change the comma "," to a semicolon --; --.

Page 4, line 8, after "SiO2", change the comma "," to a semicolon --; --.

Page 4, line 9, after "(PSG)", change the comma "," to a semicolon --; --.

Page 4, line 10, after "PSG", change the comma "," to a semicolon -- ; --.

Page 4, line 11, after "SOG", change the comma "," to a semicolon --; --.

Page 4, line 12, after "ITO", change the comma "," to a semicolon --; --.

Page 4, line 14, after "crystal", change the comma "," to a semicolon --; --.

Page 4, line 15, after "ITO", change the comma "," to a semicolon --;--.

Page 5, line 9, change "(light shielding metal layer, etc.) to -- (i.e., a light shielding metal layer, and so forth) --.

Page 6, line 8, delete "it is needles to say that".

Page 6, line 24, before "quartz" insert -- a --.

Page 7, line 1, before "second" insert -- i.e., a --; and change "DOPOS (a" to -- DOPOS, in which a --.

Page 7, line 3, change "them)." to -- them. --.

Page 7, line 13, after "line" insert -- 4 --.

Page 7, line 21, delete "this film is".

Page 8, line 6, change "runs" to -- extends--.

Page 8, line 10, after "Vcom" insert a comma --,--.

Page 8, line 18, after "film" insert -- 1 --.

IN THE CLAIMS

Please add the following new claims:

4. (newly-added) A liquid crystal display device, comprising:

a first substrate and a second substrate opposite said first substrate with a liquid crystal layer held between said first and said second substrate;

a light shielding film formed on said first substrate;

a pixel transistor formed of a first silicon layer on said first substrate, said light shielding film for shielding against incident or scattered light;

a gate line;

a capacitance line, said capacitance line and said gate line formed of a second silicon layer;

a gate insulating film;

said light shielding film formed substantially beneath said first silicon layer and extending so as to terminate at a location which is not beneath said gate line, and disposed under said capacitance line, said light shielding film being connected to a fixed potential so that an increase in parasitic capacitance between the light shielding film is suppressed, a load amount on said gate line is suppressed and a delay of gate potential is small.

5. (newly-added) The liquid crystal display device as set forth in claim 4, wherein said first silicon layer is located beneath said capacitance line and spaced from said light shielding film by a first insulating layer and substantially in register with said light emitting film at a location not beneath said gate line.

6, (newly-added) The liquid crystal display device as set forth in claim 5 wherein said

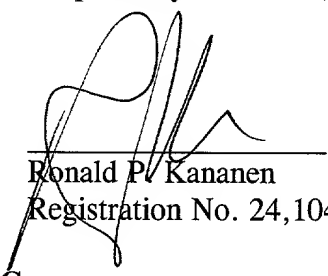
light shielding film is made from a metal and is connected to a metal layer having a fixed potential.

REMARKS

This Preliminary Amendment is requested to add additional claims in an alternate form for the initial examination, and to make minor changes in the specification as filed. No new matter has been added. Entry of this amendment is requested.

Respectfully submitted,

DATE: August 25, 1999



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# LIQUID CRYSTAL DISPLAY DEVICE

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to a liquid crystal display device, and particularly to a liquid crystal display device provided with a thin film transistor formed on a substrate.

### 2. Description of the Related Art

Hitherto, there is known a liquid crystal display device in which a thin film transistor is formed on a substrate made of, for example, glass or quartz (Japanese Patent Unexamined Publication No. Hei. 5-150262, No. Hei. 5-257164, No. Hei. 10-70277, etc.). The thin film transistor (hereinafter properly referred to as TFT) functions as a display electrode.

A conventional device of this kind, for example, a liquid crystal display device formed of a p-Si (polysilicon) thin film transistor, an a-Si (amorphous silicon) thin film transistor, or the like has a problem that such a phenomenon occurs that an off current of a pixel transistor is increased by light incident from the side of a substrate (quartz substrate, etc.) or scattered light incident from the opposite side of the substrate, and a pixel potential leaks. This phenomenon has a large tendency to occur especially in the case where the liquid crystal display device is used for a projector.

For the purpose of avoiding the phenomenon, in the related

art, as shown in a plane structure of Fig. 1 and sectional structures of Figs. 2 and 3, a metal layer made of, for example, W or its silicide which does not transmit light, is disposed as a light shielding film just under a pixel transistor. A peripheral portion of the light shielding film, for example, the metal layer is connected to a fixed potential of Vss, Vcom, or the like. Although not shown, for the purpose of blocking off scattered light incident from the opposite side of the substrate, contrary to Figs. 2 and 3, there is such a case that a metal layer of, for example, Ti which does not transmit light, is disposed as a light shielding film just over a pixel transistor, and its peripheral portion is likewise connected to a fixed potential of Vss, Vcom, or the like.

However, in such a connection method of the metal layer in the related art, the delay of a gate line potential is caused by parasitic capacitance constituted by the metal layer of the light shielding film with the fixed potential and a gate line for controlling the pixel transistor, which is made of, for example, doped polysilicon (DOPOS). As a result, such disadvantage is caused that the contrast of a liquid crystal display is lowered, or uniformity is deteriorated.

The structure and the problem of the related art will be further explained with an example of a case where the light shielding film is disposed just under the pixel transistor and with reference to Figs. 1 to 3. Fig. 1 is a view showing the

related art in the plane structure of a portion including the metal layer forming the light shielding film and a data line, Fig. 2 is a sectional view taken along line A-A' of Fig. 1, and Fig. 3 is a sectional view taken along line C-C' of Fig. 1.

As shown in Figs. 1 to 3, pixel transistors 22 and 24 are constituted by first silicon layers 21 and 23 made of, for example, undoped silicon formed on a substrate 10 (here, quartz substrate), and a gate line 3 (second silicon layer) made of, for example, DOPOS (a gate insulating film 31 made of, for example, SiO<sub>2</sub> intervenes between them). As mentioned above, since it is necessary to shield the pixel transistors 22 and 24 against light, as shown in Fig. 2, a metal layer made of, for example, W or its silicide is provided as a light shielding film 1 at the side of the substrate 10 here. This light shielding film 1 is shown especially by fine dots in Fig. 1. As shown in the drawings, this light shielding film 1 is connected to a metal layer 7 made of, for example, Al, having a fixed potential such as V<sub>ss</sub> or V<sub>com</sub> and the light shielding film 1 is formed just under the gate line 3 in the related art of this case. The gate line 3 and an additional capacitance line are formed of a second silicon layer made of, for example, DOPOS, and are especially shown by oblique lines in Fig. 1.

As described above, in the related art, since the light shielding film 1 connected to the metal layer 7 with the fixed potential is formed close to the gate line 3, the delay of the

gate line potential is caused by the parasitic capacitance formed of the metal layer 7 with the fixed potential and the gate line 3, and a problem resulting from this can occur.

Incidentally, in Figs. 1 to 3, reference numeral 6 denotes a second contact, 8 denotes a first contact, 51 and 52 denote data lines made of, for example, Al, 9 denotes an opening portion, 11 denotes a first insulating layer made of, for example, TEOS-SiO<sub>2</sub>, 12 denotes a second insulating layer made of, for example, phosphorus-containing silicon glass (PSG), 13 denotes a third insulating layer made of, for example, PSG, 14 denotes a flattened film made of, for example, SOG, 15 denotes a transparent electrode layer made of, for example, ITO, 16 denotes a liquid crystal layer made of, for example, twisted nematic (TN) liquid crystal, 17 denotes an opposite substrate side transparent electrode layer made of, for example, ITO, and 18 denotes an opposite substrate made of, for example, quartz.

#### SUMMARY OF THE INVENTION

The present invention has been made to solve the foregoing problems, and an object of the invention is to provide a liquid crystal display device including a light shielding film with a structure capable of avoiding a gate line delay.

In a liquid crystal display device including a thin film transistor formed on a substrate, the liquid crystal display device of the present invention is characterized in that a light

shielding film for shielding against light incident from the side of the substrate or scattered light incident from the opposite side of the substrate is disposed such that its portion except a portion for shielding a pixel transistor is disposed over or under an additional capacitance line or between a gate line and the additional capacitance line and at a position avoiding the gate line.

According to the present invention, the portion of the light shielding film (light shielding metal layer, etc.) except the portion shielding the pixel transistor is not disposed close to the gate line. The structure of such arrangement makes it possible that the problem of the parasitic capacitance be reduced, the load of a gate line driving transistor be reduced, and the delay of a gate pulse be suppressed.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a view showing a conventional structure in a plane structure.

Fig. 2 shows the conventional structure in a sectional structure and is a sectional view taken along line A-A' of Fig. 1.

Fig. 3 shows the conventional structure in a sectional structure and is a sectional view taken along line C-C' of Fig. 1.

Fig. 4 is a view showing a first embodiment of the present

invention in a plane structure.

Fig. 5 shows the first embodiment of the present invention in a sectional structure and is a view taken along line D-D' of Fig. 4.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described in detail below with reference to the drawings. However, it is needless to say that the present invention is not limited to the embodiments described below and shown in the drawings, but can be suitably applied to a structure having the same effect, for example, a structure in which a light shielding film is disposed over a pixel transistor.

##### Embodiment

The structure of this embodiment is shown in Fig. 4 showing a plane structure (corresponding to Fig. 1 showing the related art) and in Fig. 5 showing a sectional structure (corresponding to Fig. 3 showing the related art). Although this embodiment is a liquid crystal display device having almost the same structure as that shown in Figs. 1 to 3, the structure of a light shielding film 1 is different. Reference numerals in Figs. 4 and 5 correspond to those shown in Figs. 1 to 3.

As shown in Figs. 4 and 5, a pixel transistor 22 is formed of a first silicon layer 21 of, for example, undoped silicon formed on a substrate 10 (here, quartz substrate) and a gate

line 3 (second silicon layer) made of, for example, DOPOS (a gate insulating film 31 made of, for example, SiO<sub>2</sub> intervenes between them). As described above, since it is necessary to shield the pixel transistor 22 against light, as shown in Fig. 5, a metal layer made of, for example, W or its silicide is provided as the light shielding film 1, in this case at the side of the substrate 10 here. This light shielding film 1 is shown especially by fine dots in Fig. 5. As shown in the drawing, this light shielding film 1 is connected to a metal layer 7 made of, for example, Al and having a fixed potential such as V<sub>ss</sub> or V<sub>com</sub>. In the related art of this case, the light shielding film 1 is formed just under the gate line 3. The gate line 3 and an additional capacitance line are respectively formed of a second silicon layer made of, for example, DOPOS, and are especially shown by oblique lines in Fig. 4 as well.

In this case, as a portion to be shielded, a portion just under the thin film pixel transistor made of, for example, p-Si is inevitable, and as other portions, it is sufficient if only a part of the periphery of the pixel transistor is shielded against oblique light. Thus, in this embodiment, the light shielding film 1 (this film is formed of a light shielding metal layer made of, for example, W or its silicide, and is shown by fine dots similarly to the foregoing) has a structure as described below. That is, such a structure is adopted that the light shielding film 1 hardly exists just under the gate line

3 made of, for example, DOPOS. Specifically, the light shielding film 1 is disposed in such a manner that it avoids the gate line 3 and its portion corresponding to the gate line 3 is cut away. For example, in a section taken along line D-D' in the portion designated by B in Fig. 4, such a structure is made that the light shielding film 1 runs while avoiding the gate line 3 as shown in the drawing.

For the connection between adjacent pixels or to the peripheral metal layer 7 made of, for example, Al, and having a fixed potential of Vss or Vcom the light shielding film 1 is disposed under the additional capacitance line 4 made of, for example, DOPOS, or as shown in the drawing between the gate line 3 and the additional capacitance line 4 (avoiding the portion under the gate line 3).

By this structure, such a structure is obtained that even when the light shielding film 1 of the light shielding metal layer or the like is connected to the fixed potential, the increase in parasitic capacitance between the film and the gate line 3 can be suppressed, the load amount of the gate line 3 can be suppressed to the minimum, and the delay of the gate potential becomes very small.

As a result, in this preferred embodiment, the improvement of contrast and uniformity can be realized, and the picture quality of the liquid crystal display device can be improved.



WHAT IS CLAIMED IS:

1. A liquid crystal display device, comprising:

a first substrate on which a pixel transistor and a light shielding film for shielding against incident light or scattered light are formed, wherein a portion of said light shielding film except its portion for shielding said pixel transistor is disposed over or under an additional capacitance line or between a gate line and said additional capacitance line and at a position avoiding said gate line;

a second substrate disposed opposite to said first substrate and with a predetermined interval; and

a liquid crystal layer held between said first substrate and said second substrate.

2. A liquid crystal display device according to claim 1, wherein said light shielding film is disposed between said substrate and said pixel transistor.

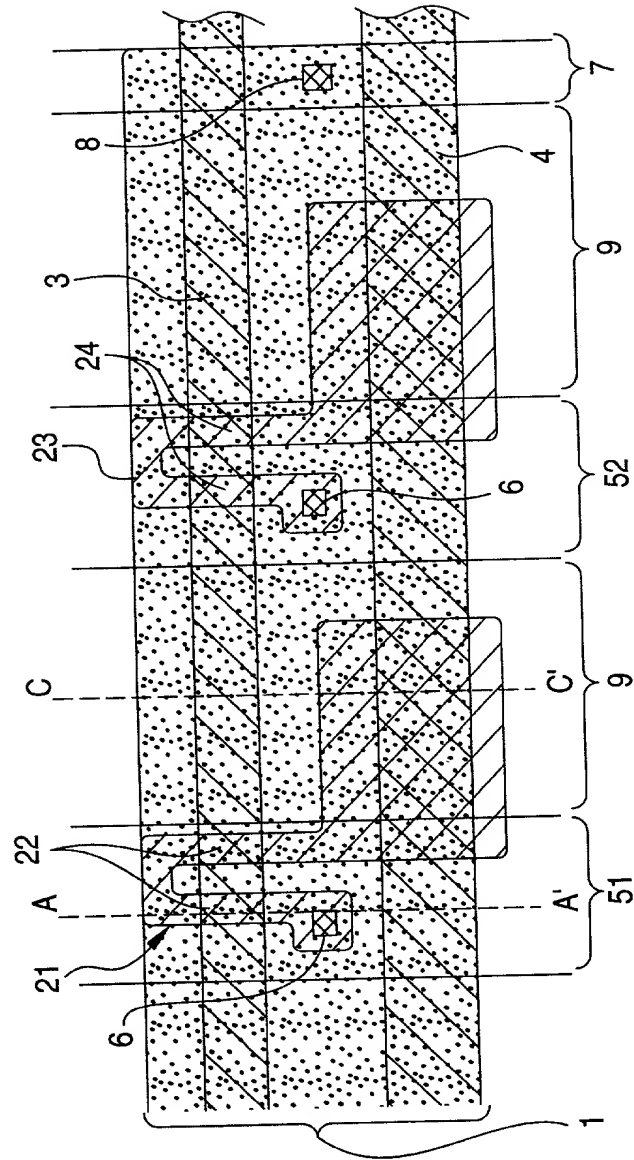
3. A liquid crystal display device according to claim 1, wherein said light shielding film is disposed over said pixel transistor.

#### ABSTRACT OF THE DISCLOSURE

In a liquid crystal display device including a light shielding film, the liquid crystal display device having a structure capable of avoiding a gate line delay is provided. In the liquid crystal display device including a thin film transistor formed on a substrate, a portion of a light shielding film for shielding against incident light from the side of the substrate, except its portion for shielding the pixel transistor, is disposed under an additional capacitance line or between a gate line and the additional capacitance line and at a position avoiding the gate line, so that parasitic capacitance between the film and the gate line is suppressed.

FIG. 1  
RELATED ART

(PLANAR STRUCTURE)



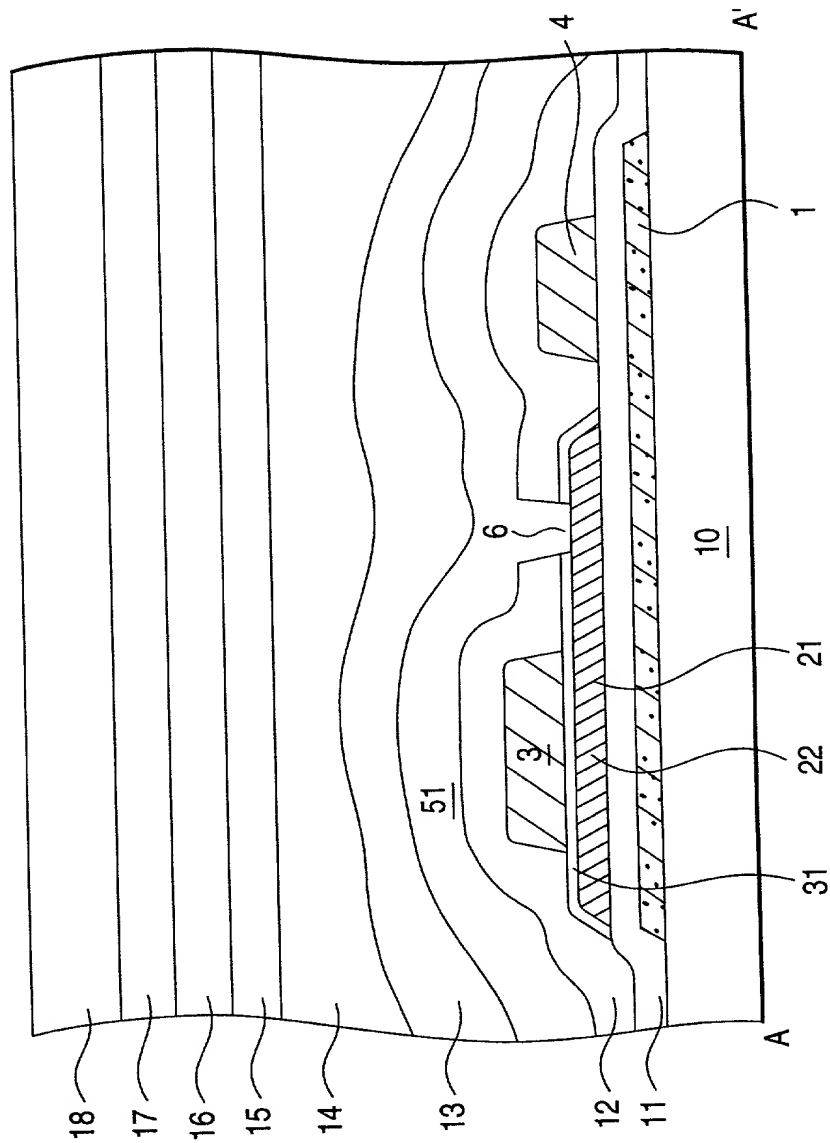
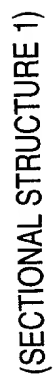
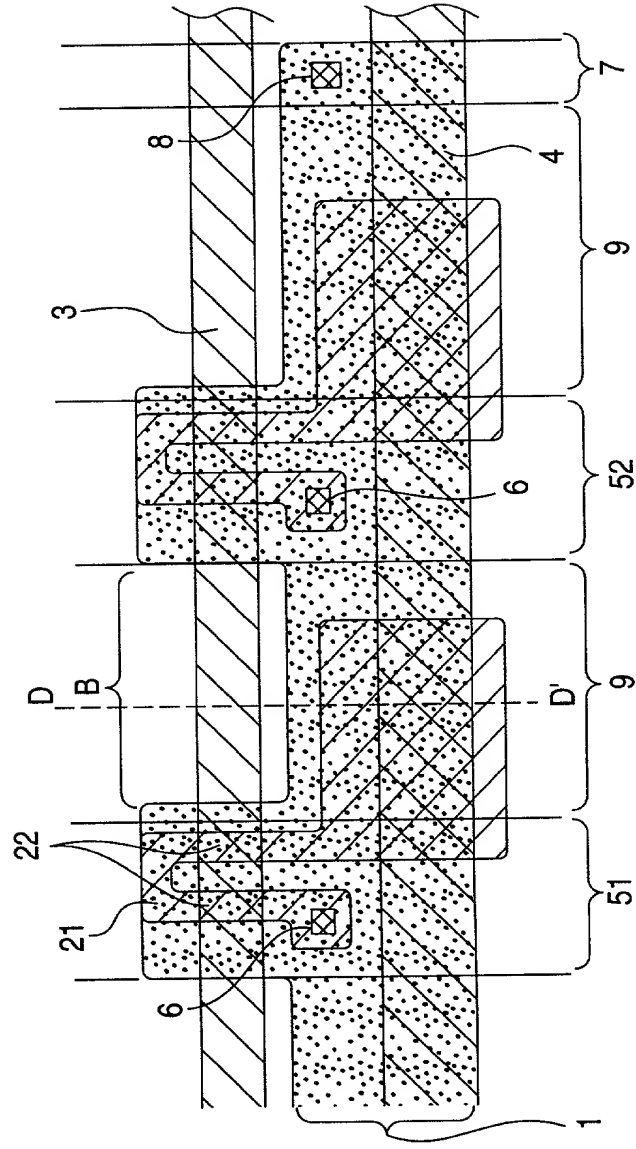




FIG. 4

STRUCTURE OF EMBODIMENT 1





Attorney's Docket No. SON-1622

**DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION**  
**English Language Declaration**

As below named inventors, we hereby declare that:

Our residence, post office address and citizenship are as stated below next to our names.

We believe we are the original, first and joint inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled

LIQUID CRYSTAL DISPLAY DEVICE

the specification of which

(check one)

X is attached hereto.

was filed on \_\_\_\_\_ as

Application Serial No. \_\_\_\_\_

and was amended on \_\_\_\_\_

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
P10-243502	Japan	28/08/1998	X	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
_____	_____	_____	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)		
_____	_____	_____	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)		

We hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 and 1.63(d) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status)
_____	_____	(patented, pending, abandoned)

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Attorney's Docket Number: SON-1622

## English Language Declaration

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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Second Inventor's signature		Date
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Third Inventor's signature		Date
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(Supply similar information and signature for subsequent joint inventors.)